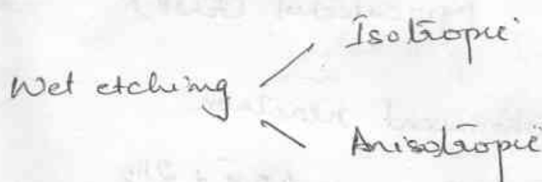
Ref: A (not so) introduction to MEMS ; F. CHOLLET, H. Liu
1b.
Date: 23/02/2015.

Bulk Micromachining:

- formation of bulk structures by removal of materials from bulk substrates.
- bulk substrate in wafer form can be silicon, glass, Quartz, crystalline Ge, SiC, GaAs, GaP or InP.
- Commonly used process - wet and dry etching. allowing varying degree of control on the profile of the final structure.

Isotropic and Anisotropic wet etching:

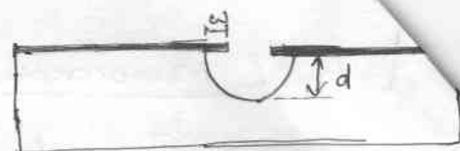
- Wet etching - immersing the material in a chemical bath that dissolves the surfaces not covered by protective layer.
- quick, uniform, very selective and cheap.
- etching rate and the resulting profile depend on the material, the chemical, the temperature of the bath, the presence of agitation, and the etch stop technique used if any.



Isotropic etching happens when the chemical etches the bulk material at the same rate in all directions, while anisotropic etching happens when different etching rate exists along different directions.

Etching rate is never zero in any specific directions and it is actually impossible to obtain etching in only one direction. This is quantified by estimating the underetch (w/d), that is the lateral etching under the edge of the mask with respect to the vertical etching

Under etch — (ω/d)

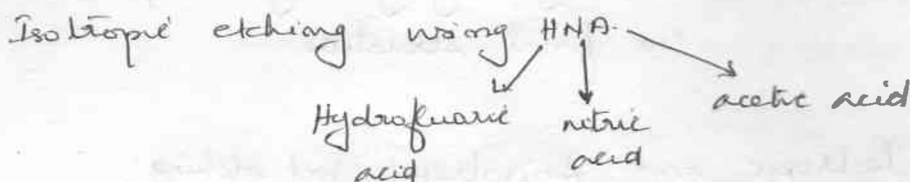


= 1 for isotropic etching

≈ 0.01 for very anisotropic etching
e.g. etching Si in KOH solution

In general acids are isotropic etchants
alkaline bases are anisotropic etchants

For Silicon.



Nitric acid act as an oxidant and HF dissolves the oxide by forming water soluble H_2SiF_6.

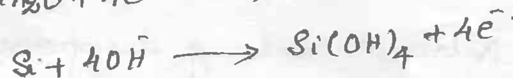
$$Si + HNO_3 + H_2O \longrightarrow SiO_2 + HNO_2 + H_2$$

$$SiO_2 + 6HF \longrightarrow H_2SiF_6 + 2H_2O$$

Anisotropic etching — KOH solution, tetramethyl ammonium hydroxide (TMAH) and ethylene diamine pyrocatechol (EDP)

Simplified chemical reaction

$$4H_2O + 4e^- \longrightarrow 4OH^- + 2H_2$$



$$Si + 4OH^- \longrightarrow Si(OH)_4 + 4e^-$$

Here, electrons are important elements in the reaction. Different crystal planes ~~[struck-out text]~~ have different density of atoms and hence of electrons.

Etch rate ratio between (100) and (111) planes – 400 (1 μm/min → 2.5 nm/min)
(100) (111)
(110) and (111) planes – 600.

Hence (111) plane is usually excellent for ~~its~~ control of the lateral etching. However, this requires proper alignment of the etch mask with respect to the planes.

Vertical etching control :- monitor the etch time.

- electrochemical etch stop - create a diode junction by using epitaxial growth or doping of a n-layer over a p-substrate. The junction is reverse polarized by contacting the substrate and the electrochemical bath, preventing current to flow between anode and cathode. As soon as the p-substrate is completely etched, a current can flow from the anode causing the apparition of a passivation layer by anodization, effectively stopping the chemical reaction and the etching.

- doping heavily the surface of silicon with boron by diffusion or implantation. As soon as the p+ doped zone is exposed the electron density is lowered slowing down the etching reaction by atleast one order of magnitude.

for instance for piezoresistive material, by ion implantation dope layers a few micrometer beneath the surface, leaving a thin top layer untouched for the fabrication of piezoresistors.

Generally, strong alkaline bases require a hard masking material that can withstand the solution without decom-posing or peeling.

For.e.g. SiO_2 mask for TMAH.

SiN_x - mask for KOH.

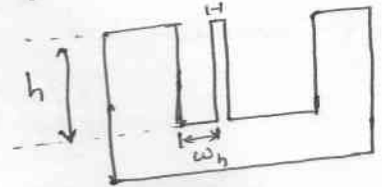
Limitations :

- Most serious one lies with the need to align the sides of the pattern with the crystal axes to benefit from the (111) plane etch-stop, severly constraining the freedom of layout.

Dry etching:

- series of subtracting methods where the solid substrate is removed by gaseous species.

Aspect ratio (h/w_r) for features



(h/w_h) for holes.

Typical values ~ 1 for isotropic etching
~50 for anisotropic etching (DRIE)

Often makes use of plasma - equal mixture of positive ions and high energy electrons with some neutral atoms that remain mostly electrically neutral.

- plasma forms high quantity reacting ions and radicals, increasing the etch rate.

Etching by three different methods

(1). Physically by ion bombardment - kicking out atoms from the surface - anisotropic, non-selective.

(2). by combining both physical and chemical effects (reactive ion etching) - anisotropic, selective

(3) ~~by~~ chemically by reaction giving gas by-products at the surface. (plasma etching or radical etching).
- isotropic, selective.

Wafer Bonding: an assembly technique where two or more precisely aligned wafers are bonded together. Used for device fabrication and also for its packaging.

main parameters :- the bonding temperature. High temp. may damage materials or structures on processed wafer

- the difference in coefficient of thermal expansion between bonded materials
- the permeability to gas and humidity of bond and bonded wafer.

Bonding techniques
- Intermediate layer bonding
- Direct bonding.

Intermediate Layer bonding.

(1) - Simplest epoxy - cures at low temp. (<100°C). and is cheap
- poses performance problem - has large thermal expansion coefficient and are permeable to gas and moisture

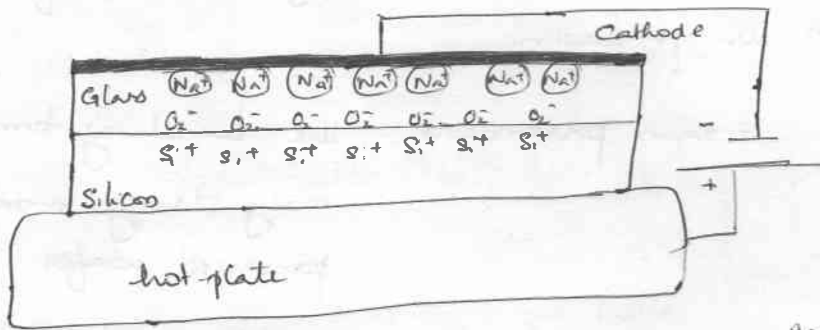
(2). Eutectic bonding :- forming an eutectic alloy that will diffuse into target wafer and form inter metallic to create a strong bond.

For Si-to-Si - gold is intermediate layer.

temp - 363°C

Direct Bonding: Most commonly used MEMS bonding method.

(1) anodic bonding :- field assisted bonding
- for bonding Si wafers with glass wafers.



→ Apply high voltage at elevated temp. (250 - 400°C)

→ Na^+ ions migrate from softened glass towards cathode

Leaving negative space charge of oxygen ions.

→ This ion repels free electrons in semiconductor, letting positive ch[arge]

appear close to the interface.

→ Strong E-field between silicon and glass pulling both s[urfaces]

to contact

→ At elevated temp. forming chemical bond with a thin layer of

Limitations :

→ Induces high stress.

Wafer bonding is also used to fabricate MEMS substrates such [as]

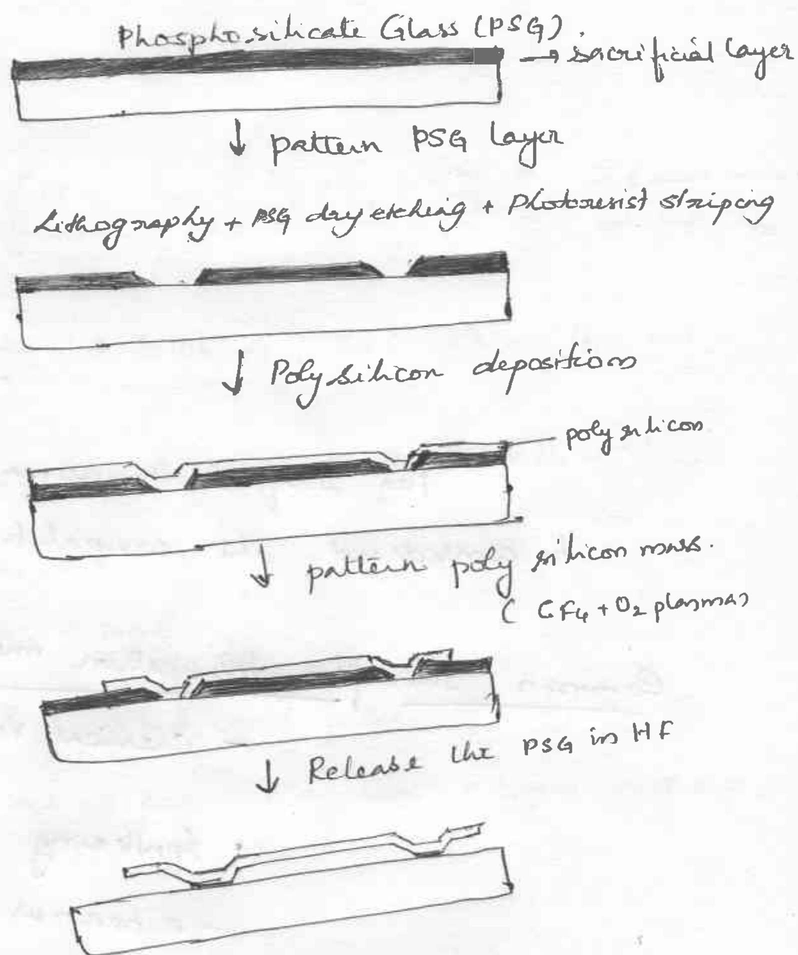
SOI or SOG (Si on glass).

Surface micromachining and thin films:

- Builds up structures by adding materials layer by layer on the surface of the substrate.

- Typically 1-5 μm thick.
- Some as structural layers and some as sacrificial layer

A typical process →



- Variety of large materials such as polysilicon, oxide, nitride, PSG, metals, diamond, SiC, and GaAs can be deposited as thin film and many layers stacked

- Allows very complicated microstructures.

Thin-film fabrication:

Important factors:
- temperature budget (limited by the maximum temperature the substrate can withstand and the allowable thermal stress).
- the magnitude of the residual stress in the thin film (Too much stress causes layer cracking)
- the conformality of thin film (how the thin-film follows the profile of the substrate
- the roughness of the thin-film
- the existence of pin-hole
- the uniformity of the thin-film
- the rate of fabrication.

• For surface micromachining, an additional factor should be considered - the compatibility between sacrificial and structural layers

Common thin-film fabrication methods:

- chemical Vapor Deposition
  - at atmospheric (APCVD)
  - at low pressure (LPCVD)
- Sputtering
- e-beam or thermal evaporation

} Physical vapor deposition

- Spin coating.
- Oxidation.

Oxidation:
- a reactive growth technique, used mostly on silicon where silicon dioxide is obtained with a chemical reaction with a gaseous flow of dry or wet dioxygen.
- dry dioxygen - slower growth rate than when water vapor are added
- But higher quality films (dry oxygen)

The rate of growth is given by

$$d_0 = \frac{A}{2}\sqrt{1+\frac{t+\tau}{A^2/4B}} - \frac{A}{2}$$

B = parabolic rate constant

B/A = linear rate constant obtained for the long and the short growth time limit

τ = correcting factor

Now when $t \to 0$, $\lim_{t \to 0} d_0 = \frac{A}{2}\left(1 + \frac{1}{2}\frac{t}{A^2/4B}\right) - A/2 = \frac{B}{A} t$ → linear in time with slope B/A.

Typical values at 1000°C are $A = 0.165\,\mu m$, $B = 0.0117\,\mu m^2/h$ and $\tau = 0.37h$ in dry O_2.

$A = 0.226\mu m$, $B = 0.287\,\mu m^2/h$ and $\tau = 0$ in wet O_2.

Model breaks down for thin dioxide $< 300 Å$

Local Oxidation: Using Si_3N_4 deposited and patterned on the silicon surface to act as barrier against oxygen diffusion.

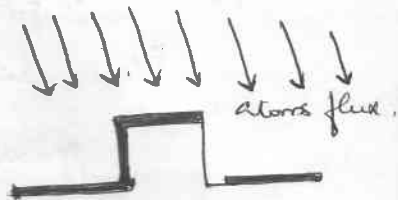
Spin-coating:

- Simple and fast technique
- used to deposit polymer in solvent (particularly photoresist)

Physical Vapor Deposition:

- evaporation and sputtering
- low temperature, good conducting materials (Au, Pt, Ti, Cr, Al, Ni)
- can be used for oxide or semi-conductive materials.

Principle of evaporation:



- wafer + source material in a vacuum chamber.
- Source material heated above its evaporation temp. sending vaporized atoms across the chamber.
- The atoms condense on the cooler surface. (wafer and chamber wall).
- material heated using resistive heating (Joule heating) or by electron beam.

E-beam -- High velocity beam of electrons directed towards the source material

- electrons collide with surface atoms -> transfer their K.E
- brings the material to high temp.
- can reach much higher temp. than resistive heating.

- For both heating techniques the surface substrate has to be kept at a relatively large distance from heating uncontrollably.
- large distance results in line of sight deposition with poor conformality i.e. horizontal surface uniformly coated while vertical surface will receive less materials as their projected surface is smaller